Remarks

In the Office Action, the Examiner noted that claims 1-34 are pending in the application, and that claims 1-34 are rejected. By this amendment, claim 21 has been amended. Thus, claims 1-34 are pending in the application.

Applicant hereby requests further examination and reconsideration of the application, in view of the foregoing amendments.

In the Declaration

Applicant notes the Examiner's indication that the declaration as originally submitted is defective because the title reflected in the declaration does not match the title in the specification. Enclosed herewith is a declaration with the proper title executed by the inventors prior to preparation of the instant Amendment.

In the Specification

The Examiner requested Applicant's assistance in correcting the specification. The specification incorporates by reference three patent applications which have since issued into U.S. Patents. Hence, the specification has been amended herein to refer to the issued patents.

In the Drawings

The Examiner objected to Fig. 4 as failing to comply with 37 CFR 1.84(p)(5) because it included a reference sign to element 416 not mention in the description. The specification has been amended to refer to element 416. The Examiner objected to the fact that the specification states there are Figures 1 through 8, however Figures 5 through 8 were not present. Figures 5 through 8 are described in detail in the disclosure; however, the drawings of Figures 5 through 8 were not included in the original filing through inadvertence. The drawings of Figures 5 through 8 have been included in the drawings submitted herewith to secure substantial correspondence between the specification and the drawings in accordance with 37 CFR § 1.121(e). No new matter has been added since Figures 5 through 8 are fully described in the originally filed specification at page 38, line 7 through page 48, line 23. The Examiner required that

Figure 1 be corrected so that the reference numeral "157" is on one line. The correction has been made. Applicant herewith submits a Transmittal of Formal Drawings to the Official Draftsman.

In the Claims

Rejection Under 35 USC 112 second paragraph

The Examiner rejected claim 21 under 35 U.S.C. § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Applicant has amended claim 21 to remedy the drafting error.

Rejection Under 35 USC 102(b)

The Examiner rejected claims 1-6, 8-20 and 26-29 under 35 U.S.C. § 102(b), as being unpatentable over *Abramson et al.*, U.S. Patent No. 5,606,670 (hereinafter *Abramson*). Applicant respectfully traverses.

Broadly speaking, *Abramson* is directed to an out-of-order execution microprocessor that includes store forwarding circuitry. *Abramson* discloses a store buffer with multiple buffer slots that buffer data and addresses of data store operations. Col. 4, lines 63-65; col. 5, lines 51-54. The store forwarding circuitry conditionally forwards store data from a subset of the store buffer slots for a load operation based on the time the load operation is issued. Col. 7, lines 38-44.

With respect to claim 1, the Examiner asserts that *Abramson* teaches a result forwarding cache (RFC). Applicant respectfully asserts that *Abramson* does not teach an RFC. As disclosed in Applicant's instant Application, an RFC is an array of storage elements, each of which stores an instruction result and information specifying a destination register of the result. See col. 14, lines 14-17, 25-32, 52-67 and col. 15, lines 1-27 of U.S. Patent 6,343,359, which incorporated by reference at page 2, lines 7-10 of the instant Application. Applicant's instant disclosure teaches an RFC that has been modified to advantageously store not only instruction results destined for microprocessor registers, but also store instruction results destined for memory. Page 24, line 19 to page 25, line 2. The Examiner asserts that *Abramson* teaches an RFC at column 2, lines 36-43 and

columns 4-5, lines 56-7. The cited text of *Abramson* teaches the store buffer with multiple buffer slots mentioned above. *Abramson* teaches the store buffer stores store instruction results destined for memory. However, Applicant can find no teaching in *Abramson* in which the store buffer stores instruction results destined for a microprocessor register. Hence, Applicant respectfully asserts the cited text of *Abramson* does not teach an RFC, nor can Applicant find any teaching in *Abramson* of an RFC. Therefore, *Abramson* does not anticipate claim 1.

With respect to claim 10, the Examiner asserts that *Abramson* teaches an RFC configured to forward a first plurality of store instruction results, and a data unit configured to forward a second plurality of store instruction results. Applicant respectfully asserts that *Abramson* does not teach an RFC for the reasons stated above with respect to claim 1. Furthermore, Applicant respectfully asserts that *Abramson* does not teach selection logic that selectively provides one of a first plurality of store instruction results from an RFC and a second plurality of instruction results from a data unit to a stage of the microprocessor pipeline executing a load instruction, as recited in claim 10. Applicant points out that the Examiner refers to the same structure in *Abramson*, namely *Abramson*'s store buffer, as teaching both the RFC and as teaching the data unit recited in claim 10. However, claim 10 specifically recites selection logic that selects either the store instruction results from the RFC or the store instruction results from the data unit to forward to the load instruction. The selection logic of *Abramson* selects between one of multiple buffer slots in the store buffer to forward (col. 7, lines 39-45; col. 8, lines 2-6; col. 10, lines 60-67; col. 11, lines 26-29), not between the store buffer and an RFC to forward store instruction results. In contrast, the selection logic as recited in claim 10 selects between store instruction results of the data unit and the RFC. Therefore, *Abramson* does not anticipate claim 10.

With respect to claim 18, the Examiner asserts that *Abramson* teaches first comparison logic for comparing a load instruction load address in a first stage of a microprocessor pipeline with a first plurality of store addresses of first store instruction data in a plurality of stages of the pipeline subsequent to the first pipeline stage. Applicant can find no teaching of comparison logic that compares a load instruction address with a plurality of

store addresses of store instruction data in a plurality of stages of the microprocessor pipeline subsequent to the pipeline stage of the load instruction. *Abramson* teaches address conflict detection circuitry that includes an equality comparator (element 50 of Fig. 6) that compares a load operation address with a plurality of store operation addresses. Col. 9, lines 22-25. *Abramson* also teaches a plurality of equality comparators (element 72a of Fig. 7) each of which compares a page reference portion of a linear address of a load operation to a page reference portion of a linear address of a buffered store operation and outputs a match signal with a logic one value if the two linear addresses are equal. Col. 9, line 66 to col. 10, line 3. The plurality of store operation addresses are stored in buffer slots of a store buffer. Col. 6, lines 4-6. Hence, *Abramson* may teach the second comparison logic element of claim 18; however, Applicant can find no teaching in *Abramson* of the first comparison logic recited in claim 18, which compares the load address with store addresses in a plurality of pipeline stages other than the store buffer store addresses, which are compared by the second comparison logic, as recited by claim 18. Consequently, *Abramson* also does not teach control logic that determines which of the first and second store instruction data is newest based on the comparison performed by the first and second comparison logic, since *Abramson* does not teach the first comparison logic. Therefore, *Abramson* does not anticipate claim 18.

With respect to claim 26, Applicant respectfully asserts that *Abramson* does not teach forwarding storehit data from an RFC for the reasons discussed above with respect to claim 1. Therefore, *Abramson* does not anticipate claim 26.

Applicant respectfully asserts *Abramson* does not anticipate dependent claims 2-9, 11-17, 19-20, and 27-29 because they depend from independent claims 1, 10, 18, and 26, respectively, which are not anticipated by *Abramson* for the reasons discussed above.

Rejection Under 35 USC 103

The Examiner rejected claims 21-25 and 30-34 under 35 U.S.C. § 103 as being unpatentable over *Abramson* in view of Patterson and Hennessy's Computer Architecture: A Quantitative Approach, Second Edition © 1996 (hereinafter *Hennessy*). Applicant respectfully traverses the Examiner's rejections.

With respect to claim 21, the Examiner asserts that *Abramson* teaches a plurality of physical address comparators, for comparing a load address with a plurality of store addresses and generating a physical match signal. Applicant has amended claim 21 to clarify the meaning of physical address as an address translated from a virtual address. Applicant can find no teaching in *Abramson* of an apparatus for speculatively forwarding storehit data having a plurality of physical address comparators as recited in amended claim 21.

Abramson teaches a microprocessor with a memory paging system that includes translation lookaside buffers that translate a linear address into a physical address. *Abramson* also refers to the linear addresses as virtual addresses. A linear address includes a page offset portion that comprises the lower 12 bits of the linear address (apparently *Abramson* describes a system with 4KB memory pages), and a page reference portion that comprises the upper 20 bits of the linear address. The physical address comprises a page offset portion that comprises the lower 12 bits of the physical address, and a page address portion that comprises the upper 28 bits of the physical address. The page offset portion of the physical address is the untranslated page offset portion of the linear address. The page address portion of the physical address is translated from the page reference portion of the linear address. Fig. 2; Fig. 11; col. 3, line 63 to col. 4, line 10; col. 5, lines 8-13; col. 2, line 55; col. 7, lines 55-56 and col. 8, lines 7-16.

Abramson also teaches a plurality of equality comparators (element 72a of Fig. 7) each of which compares a page reference portion of a linear address of a load operation to a page reference portion of a linear address of a buffered store operation and outputs a match signal with a logic one value if the two linear addresses are equal. Col. 9, line 66 to col. 10, line 3. *Abramson* also teaches a plurality of equality comparators (element 50 of Fig. 6) that each compare the untranslated page offset portions of the load and store addresses. Col. 7, lines 53-56; col. 9, lines 23-26, 29-35. *Abramson* also teaches storage of translated physical addresses of buffered store operations in a physical address buffer. Fig. 3, element 34; col. 6, lines 9-13. However, Applicant can find no teaching in *Abramson* of physical address comparators that compare a physical load address translated from a virtual load address with a plurality of physical store addresses

translated from a plurality of virtual store addresses to generate a physical match signal, as recited in amended claim 21.

Applicant further points out that the meaning of the term "speculative" as used by *Abramson* is different from the meaning used in claim 21. *Abramson* teaches an out-of-order processor in which the execution of an instruction may be speculative because the instruction was speculatively fetched and issued based on a prediction of a branch instruction that was later determined to be mispredicted, requiring subsequent flush of the results of the speculatively executed instruction. Col. 4, lines 42-55. However, the instant application teaches and claims speculative store forwarding which is speculative because the forwarding of store data is performed based on a mismatch of virtual load and store addresses; however, a subsequent physical address comparison after the virtual addresses are translated reveals a match of the physical load and store address, referred to as a virtual aliasing condition, thereby requiring correction of the speculative store forward. Page 33, line 18 to page 35, line 24. For these reasons, *Abramson* does not obviate amended claim 21.

With respect to claim 23, the Examiner asserts that *Abramson* teaches address region logic, configured to receive the load address and generate a match signal to indicate whether the load address is within one of a plurality of non-cacheable address regions of the microprocessor stored in the address region logic. *Abramson* teaches load eligibility detection circuitry having a decoder that receives a load operation's memory type and responsively outputs a signal to indicate whether the load operation's memory type is an eligible memory type for store forwarding. Col. 10, lines 32-49. However, Applicant can find no teaching in *Abramson* of address region logic that stores a plurality of non-cacheable address regions of a microprocessor address space, and generates a match signal to indicate whether a load address is within one of the stored plurality of non-cacheable address regions.

Applicant further points out that the meaning of the term "speculative" as used by *Abramson* is different from the meaning used in claim 23. The meaning of speculative taught by *Abramson* teaches an out-of-order processor in which the execution of an

instruction may be speculative because the instruction was speculatively fetched and issued based on a prediction of a branch instruction that was later determined to be mispredicted, requiring subsequent flush of the results of the speculatively executed instruction. Col. 4, lines 42-55. However, the instant application teaches and claims speculative store forwarding which is speculative because the forwarding of store data is performed based on a match of a virtual load and store address; however, after the virtual load address has been translated into a physical address it is determined that the load physical address is to a non-cacheable region, thereby requiring correction of the speculative store forward. Page 36, lines 1-23. For these reasons, *Abramson* does not obviate claim 23.

With respect to claim 30, Applicant respectfully asserts, for the reasons discussed above with respect to claim 21, that *Abramson* does not teach detecting a virtual aliasing condition with respect to a load address and one of a plurality of store addresses based on a physical address comparison between the load address and the plurality of store addresses after speculatively forwarding storehit data from a first microprocessor stage to a second microprocessor stage based on a virtual address comparison. Therefore, *Abramson* does not obviate claim 30.

With respect to claim 34, the Examiner asserts that *Abramson* teaches determining a load address is within a non-cacheable address region subsequent to speculatively forwarding. As discussed above with respect to claim 23, *Abramson* teaches load eligibility detection circuitry having a decoder that receives a load operation's memory type and responsively outputs a signal to indicate whether the load operation's memory type is an eligible memory type for store forwarding. Col. 10, lines 32-49. Applicant can find no teaching in *Abramson* as to whether a load operation's memory type specifies whether the load address is within a non-cacheable address region. However, assuming this *arguendo*, *Abramson* teaches using the decoder output signal to not store forward if the decoder output signal is true. In contrast, claim 23 recites speculatively forwarding the storehit data, and subsequently determining the load address is within a non-cacheable address region. Therefore, *Abramson* does not obviate claim 34.

Applicant respectfully asserts *Abramson* in view of *Hennessy* does not obviate dependent claims 22, 24-25, and 31-33 because they depend from independent claims 21, 23, and 30, respectively, which are not obviated by *Abramson* in view of *Hennessy*, for the reasons discussed above.

For all of the reasons advanced above, Applicant respectfully submits that claims 1-34 are in condition for allowance. Reconsideration of the rejections is requested, and Allowance of the claims is solicited.

Applicant earnestly requests the Examiner to telephone him at the direct dial number printed below if the Examiner has any questions or suggestions concerning the application or allowance of any claims thereof.

Respectfully submitted,

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